CONCORDIA UNIVERSITY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

COEN 451/6511 VLSI Design

Project

Assigned October 22nd, 2024. Report due via Moodle, Monday Dec 2nd, 10pm

General information:

- The project accounts for 25% of this course's mark.
- The project will be carried out in teams of two, which include students of different degree level.
- Designs will be done using the TSMC 180nm technology, or another one you are familiar with.
- Performance achieved should be comparable to published work using the same technology.
- Reports will consist of two parts. The first part is a two-column paper in the IEEE template (www.**ieee**.org/documents/**TRANS**-JOUR.doc*)* outlining the interesting parts of the work, summarizing targeted specifications, analysis and optimization, and giving simulation results. Please keep it to eight pages. The second part will be an appendix in which all other simulation results/schematics etc can be placed.
- You should use hierarchy in your design, meaning that you draw a schematic for a block using VDD and Gnd globals. Define a symbol view for the schematic. Then instantiate the symbol in the higher-level schematic. Your final design should be a test bench consisting of your inputs, the dc power supply and suitable input shaping circuits and loading circuits.

Elements:

The theme for projects is Input/Output circuitry. That is, to consider getting signals into and out of chips, as well as across chips. Within this general framework, you can consider designing an SRAM memory array, a multiplier, an adder or other digital system, including a simple state machine. The I/O theme should be incorporated as follows:

1. One output will drive an off-chip load, modeled as a 50 Ohm resistor to ground in parallel with a 10 pF capacitor.
2. One signal in the design will traverse a 1 mm wire. Ideally this would be a bus of signals so coupling is considered as well.

Potential Topics:

Flip-flops:

If you decide to design a flip-flop, start by specifying a maximum input capacitance. You can do this by giving a maximum number of μm of input transistor width for each input. Specify a load capacitance in a similar way. Decide what features you will add, such as a reset (synchronous or asynchronous). Consider a use-case for the flip-flops such as a serial to parallel shift register, or a PRBS generator implemented as a linear feedback shift register.

Things to "measure" in simulation:

- Set up and hold times. Determine the minimum capturable pulse width on the D input.
- Clock to Q delay. Report for a few different loading conditions
- Power dissipation for a given clock frequency
- Report values for the schematic-level simulation and the post-layout simulation including parasitic capacitance. Discuss differences
- Show the layout and successful operation in your chosen use case

- Report the area, defined as the area per FF when they are tiled together.

You can choose from a variety of implementation styles. Please see the lecture notes and the textbook for ideas.

SRAM:
If you decide to design an SRAM array, you will be responsible for an array of SRAM cells, wordline decoders and drivers, bitline drivers for writing and buffers for reading. Write an 8-bit word at a time.

Things to measure in simulation:
- Read time
- Write time
- Energy per read
- Energy per write
- Report values for the schematic-level simulation and the post-layout simulation including parasitic capacitance.
- Report the area per cell when tiled in the array and the area overhead of the peripheral circuitry.
- The wordline and bitline circuitry is usually laid out so that it is pitch-matched to the array, thus giving you great practice in layout.

Other topics:
If there is another topic that is of interest to you, please write a paragraph describing what you want to do. E.g., an adder of a particular type, or a multiplier. Explain what specs you will target and what you plan to consider in the design.

What makes complete simulation:
- Consider different supply voltages. Nominal +/- 10%
- Different process corners
- Post-layout simulations

Schedule
You have 6 weeks for the project
- Oct 28th 11:59pm: Team selection, project selection, submission via moodle giving project plan.
- Nov 5th: Preliminary schematic/block diagram. Specification (input, output loading). Where is the long wire? There could be a comparison of topologies that are enumerated here
- Nov 12th: Cadence schematics that are sized and simulated
- Nov 19th: Thorough simulations and preliminary layout done
- Nov 26th: Layout and post-layout simulations done
- Dec 2 (Monday): Report submitted

More details on 1st deliverable:
In a single document put your names, ids, ENCS login ids, and project description. If you have thoughts already on any specs or a block diagram include it too. This is due the day before our next class, allowing me to look at them, and follow up in person the day of our next lecture. Feel free to exchange emails with the instructor before the due date to get preliminary feedback.